



# **Cross-Technology Engineering Knowledge Transfer from Semiconductor Backend to Solar Cell Manufacturing: Methodology, Process Control Adaptation, and Yield Ramp Acceleration Outcomes**

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**ABSTRACT:** The 2025 commissioning of the first fully domestic US solar cell manufacturing facility at ES Foundry in Greenwood, South Carolina marked a strategic inflection point in the North American photovoltaic supply chain. The facility was commissioned under the policy tailwinds of the Inflation Reduction Act, which created urgent commercial demand for domestically manufactured cells, but simultaneously confronted the engineering reality that no large-scale silicon solar cell manufacturing capability had operated in the United States for more than a decade. The knowledge base required to ramp such a facility to competitive yield and efficiency had to be constructed from a combination of imported talent, licensed technology, and, critically, adapted engineering practice from adjacent manufacturing disciplines.

This white paper documents the systematic cross-technology engineering knowledge transfer from semiconductor backend manufacturing to silicon solar cell production that underpinned the yield ramp of the ES Foundry facility through its first nine months of operation. The author, who brings both semiconductor fabrication engineering experience (Conexant Systems, 2005-2009) and fifteen years of solar cell manufacturing leadership (REC Solar, 2009-2024), led the cross-technology methodology adoption at ES Foundry from the facility commissioning phase in late 2024 through the stabilization achieved by October 2025. The principal findings of the knowledge transfer program are summarized in the following bullet points.

- **Yield ramp acceleration:** Line yield improved from 68% at first-silicon in February 2025 to 94% by October 2025 - a 5-month ramp versus an industry benchmark of 9-12 months for greenfield solar cell facilities.
- **Process capability achievement:**  $Cpk \geq 1.50$  achieved on 14 of 18 primary process parameters within 6 months of first-silicon, enabled by semiconductor-origin SPC architecture deployed at facility startup rather than retrofitted after ramp.
- **Equipment productivity:** Overall Equipment Effectiveness (OEE) reached 78% at month 6 and 84% at month 9, against a typical 65-70% at the equivalent lifecycle stage for conventional solar cell facility ramps.
- **Cost-per-watt trajectory:** Production cost converged to within 14% of incumbent offshore benchmark by Q4 2025, 18 months ahead of the pre-program projection.
- **Applicable methodologies transferred:** 9 distinct semiconductor manufacturing disciplines identified, prioritized, and adapted to solar cell context - from process integration discipline through failure-mode-and-effect analysis to copy-exact tool qualification.

**KEYWORDS** Knowledge Transfer · Cross-Industry Engineering · Semiconductor Manufacturing · Solar Cell Production · PERC Cell · Yield Ramp · Process Control · SPC Deployment · Copy-Exact · Process Integration · US Domestic Manufacturing · Inflation Reduction Act

## **I. CONTEXT & STRATEGIC RATIONALE**

### **1.1 The Policy and Commercial Landscape**

The passage of the Inflation Reduction Act in August 2022 fundamentally restructured the economics of domestic US solar cell manufacturing. The Advanced Manufacturing Production Credit under Section 45X established per-watt manufacturing incentives that, combined with direct investment tax credits and anticipated tariff environments on imported cells, made domestic cell manufacturing economically viable at scale for the first time since the collapse of the early-2000s US solar manufacturing base. By the end of 2022, multiple domestic cell manufacturing projects had entered

serious development, and the competitive question shifted from whether to build domestic capacity to which operator could reach competitive cost parity with offshore benchmarks first.

ES Foundry entered this competitive environment with a 1 GW planned capacity facility in Greenwood, South Carolina, designed for PERC-architecture monofacial and bifacial solar cells using M10 wafer format. The facility broke ground in June 2024, achieved tool move-in for the first GW by Q4 2024, and reached first-silicon in February 2025. The yield ramp challenge was substantial: no US-domestic cell manufacturing engineering workforce existed at scale, the global solar cell engineering talent base was concentrated in Asia, and the window of competitive advantage provided by the policy-created cost gap was understood to be time-limited as offshore manufacturers invested in their own automation and cost-reduction programs.

### 1.2 The Engineering Knowledge Gap

The engineering disciplines required to ramp a greenfield solar cell facility to competitive performance include, in decreasing order of domain specificity: silicon solar cell device physics, PERC-specific process integration knowledge, screen-printing metallization operations, PECVD and diffusion process operations, and general semiconductor-class yield engineering and process control practice. The first four categories are solar-specific; the last category is a general manufacturing discipline shared across silicon-based manufacturing industries. When the available solar-specific talent was constrained, the pragmatic engineering strategy adopted at ES Foundry was to accept that the solar-specific disciplines would be filled by a combination of licensed technology, imported expert consulting, and the inevitable learning curve, while the general semiconductor-class disciplines could be transferred from adjacent industries available in the US domestic engineering market.

The author’s personal career trajectory - four years of semiconductor backend engineering at Conexant Systems followed by fifteen years of solar cell manufacturing leadership at REC Solar - positioned him to personally bridge the translation. The cross-technology knowledge transfer program documented in this paper reflects both systematic institutional knowledge codification and personal expertise translation across the two industries.

**TABLE 1 | Engineering discipline mapping - semiconductor backend to solar cell manufacturing**

Semiconductor Practice	Solar Cell Equivalent	Transfer Maturity
Wafer-level yield learning	Cell-level yield engineering	Direct transfer
Defect density Pareto analytics	EL-based defect categorization	Adapted
Copy-exact tool qualification	Printer fleet matching protocols	Adapted
Design-of-experiments methodology	Recipe optimization DOEs	Direct transfer
Process integration teams (PIEs)	Process module engineering teams	Direct transfer
Run-to-run (R2R) control	Wafer-to-wafer recipe feedback	Adapted
SPC: Shewhart + CUSUM architecture	Inline metrology SPC framework	Direct transfer
Copy-exact qualification (CEQ)	Fleet-wide tool baselining	Adapted
Failure-mode-and-effect analysis (FMEA)	Cell-level PFMEA	Direct transfer
Statistical tool matching	Inter-tool variance reduction	Adapted

The transfer maturity classification in Table 1 reflects whether each discipline could be applied without substantive modification (Direct transfer) or required specific adaptation to solar cell context (Adapted). Of the 10 disciplines

catalogued at the program outset, 5 were classified as directly transferable and 5 required adaptation - a ratio that itself informed the program structure and resource allocation.

## II. METHODOLOGY FRAMEWORK

### 2.1 The Three-Phase Transfer Model

The knowledge transfer program was structured as a three-phase model inspired by the institutional transfer frameworks used in semiconductor fab-to-fab technology transfers. The three phases, executed sequentially with partial overlap, are described in the following enumeration.

**1. Phase One - Codification.** The author and a small team of imported semiconductor-industry engineering advisors documented the semiconductor disciplines in a set of internal engineering standards tailored to the ES Foundry context. This codification phase produced approximately 340 pages of internal engineering practice documents covering all 10 disciplines identified in Table 1, executed over the period October 2024 through January 2025.

**2. Phase Two - Adaptation.** Each codified discipline was then evaluated against the specifics of solar cell manufacturing and adapted where the semiconductor version would not transfer cleanly. The adaptation work spanned January through April 2025 and produced discipline-specific adaptation notes covering solar-specific variations in process parameters, metrology capabilities, equipment architectures, and product-quality definitions.

**3. Phase Three - Deployment.** The adapted disciplines were formally deployed into the ES Foundry production organization through a structured rollout covering engineer training, SOP release, tool qualification, and first-production-lot application. Phase Three spanned February through October 2025 and was the phase during which the measurable yield, OEE, and cost outcomes were achieved.

### 2.2 Discipline-Level Adaptation Priorities

Within the portfolio of 10 disciplines, the adaptation priority was determined by two criteria: the criticality of the discipline to the yield ramp trajectory, and the magnitude of adaptation required to render the semiconductor practice usable in the solar context. These two dimensions were mapped to a priority tier classification that governed resource allocation across the adaptation phase.

TABLE 2 | Adaptation priority tier classification for the 10 transferred disciplines

Discipline	Criticality	Adaptation Effort	Priority Tier
Yield engineering (Cell-level)	Very High	Low	Tier 1
SPC architecture deployment	Very High	Low	Tier 1
Copy-exact tool qualification	High	Medium	Tier 1
Process integration discipline	Very High	Medium	Tier 1
EL-defect categorization system	High	High	Tier 2
Run-to-run (R2R) control	Medium	High	Tier 2
Printer fleet matching	High	Medium	Tier 2
DOE-based recipe optimization	High	Low	Tier 2
Cell-level PFMEA	Medium	Low	Tier 3
Inter-tool variance reduction	Medium	Medium	Tier 3

The four Tier 1 disciplines were targeted for deployment within the first 60 days of first-silicon, ensuring that the yield ramp began with the highest-leverage semiconductor-origin disciplines already operational rather than being retrofitted after production instability had manifested. The four Tier 2 disciplines were targeted for deployment between days 60 and 120, and the remaining disciplines between days 120 and 180. This time-phased rollout is one of the strongest single determinants of the accelerated ramp outcome, as discussed in Section IV.

### 2.3 Resource Allocation and Team Composition

The engineering team responsible for executing the knowledge transfer program was structured as a hybrid team combining domain expertise imported from semiconductor backend, domain expertise recruited from solar cell manufacturing, and a core of general manufacturing engineering talent recruited from the US domestic engineering market. The team composition by discipline origin is summarized as follows.

- **Semiconductor-origin engineers:** 6 senior engineers and 11 mid-level engineers recruited from US semiconductor backend fab operations (specifically: Texas Instruments Richardson, GlobalFoundries Malta, Intel Chandler, and Conexant Newport Beach). These engineers provided the semiconductor practice codification and adaptation capability.
- **Solar cell origin engineers:** 4 senior engineers and 7 mid-level engineers recruited from international solar cell manufacturing operations (predominantly Malaysia, Taiwan, and Singapore). These engineers provided solar-specific process knowledge and verified the adaptation outputs against solar cell reality.
- **General manufacturing origin engineers:** 22 engineers at entry and mid-level from US engineering graduate programs and from adjacent US manufacturing industries (automotive, aerospace, general electronics assembly). These engineers provided the bulk operational execution capacity.
- **Executive sponsorship:** The program was sponsored at VP-Technology and COO level, with a weekly steering committee that included the facility general manager, the VP of engineering, the VP of manufacturing operations, and the author as knowledge transfer program director.

#### ► STRATEGIC OBSERVATION

The single most impactful staffing decision in the knowledge transfer program was the deliberate inclusion of semiconductor-industry engineers despite their lack of solar cell domain knowledge. The solar cell industry worldview tends to regard semiconductor practice as over-engineered for the throughput-cost trade-off of solar manufacturing; the semiconductor industry worldview tends to regard solar cell practice as under-disciplined compared to leading-edge semiconductor standards. Both worldviews contain truth. Bringing both into the same organization - under explicit shared ownership of the yield ramp outcome - proved to be the structural condition that enabled the successful knowledge translation.

### III. THE NINE TRANSFERRED DISCIPLINES

This section describes, in turn, each of the nine transferred engineering disciplines. For each discipline, the section documents: the semiconductor origin practice, the adaptation made for solar cell context, the deployment timeline at ES Foundry, and the measurable impact on the yield ramp trajectory.

#### 3.1 Discipline 1 - Yield Engineering at the Cell Level

##### ▸ Semiconductor Origin

In semiconductor backend manufacturing, yield engineering is a formally defined function with dedicated engineering headcount whose responsibility is the systematic identification, categorization, and elimination of wafer-level defect sources. The yield engineer operates on a weekly cadence of defect Pareto analysis, drill-down to specific defect categories, correlation to process-step origin, and sign-off on corrective action. The semiconductor yield engineer works across multiple product designs and is trained to think in terms of per-die defect density rather than per-wafer aggregates.

##### ▸ Solar Cell Adaptation

The solar cell analog of wafer-level yield engineering is cell-level yield engineering, and the direct translation was largely successful with three adaptations: the defect categorization taxonomy was adapted from semiconductor defects (particles, void, bridge, open, short, etch residue) to solar-cell defects (chip, crack, contact-open, metallization-defect, encapsulation-defect); the measurement modalities shifted from optical and SEM inspection to electroluminescence imaging, infrared thermography, and flash test parametric; the per-cell defect density metric was translated to cell-level yield loss rate in percentage rather than defects-per-cm<sup>2</sup>.

##### ▸ Outcome at ES Foundry

The yield engineering function was stood up within 30 days of first-silicon with three dedicated yield engineers reporting directly to the VP of Engineering. Within 90 days of first-silicon, the yield engineering team had established a weekly Pareto review cadence, a defect-categorization database populated by EL-image analysis, and a corrective action tracking system. The measurable impact is documented in Section IV; most visibly, the line yield trajectory from 68% at first-silicon to 94% at month 5 was substantially faster than the industry benchmark for comparable greenfield ramps.

### 3.2 Discipline 2 - SPC Architecture Deployment

#### ▸ Semiconductor Origin

The semiconductor industry has refined SPC practice over four decades of production engineering. The canonical architecture combines Shewhart X-bar and R charts with 3-sigma action limits for large-shift detection, cumulative sum (CUSUM) charts with carefully calibrated reference values and decision thresholds for small-drift detection, and run-to-run (R2R) feedback control for automatic process adjustment based on downstream parametric metrology. The architecture is deployed at every significant process step and is integrated with the manufacturing execution system to provide real-time process state visibility and automatic alert dispatch.

#### ▸ Solar Cell Adaptation

Solar cell manufacturing historically relied on less sophisticated SPC, frequently limited to daily or shift-cadence aggregated control charts rather than wafer-level real-time monitoring. The adaptation for ES Foundry deployed the full semiconductor architecture in solar context, with metric-set adaptation to solar-relevant parameters: Etch surface reflectance, PECVD film thickness, diffusion sheet resistance, silver paste linewidth and height, and implied open-circuit voltage replaced the semiconductor metrics of critical dimension, overlay, and dopant implant dose.

#### ▸ Outcome at ES Foundry

The SPC architecture was deployed in two waves: wave one covered the Tier 1 critical process steps (Texture, diffusion, PECVD and metallization) with full Shewhart and CUSUM coverage completed by day 45 after first-silicon; wave two covered the Tier 2 steps (edge isolation, Selective emitter, firing, and flash test) completed by day 90. The rapid Cpk trajectory documented in Section IV.2 is largely attributable to the SPC deployment being in place before yield excursions could accumulate into lot-level loss.

### 3.3 Discipline 3 - Copy-Exact Tool Qualification

#### ▸ Semiconductor Origin

Copy-exact qualification is the semiconductor industry discipline of requiring every tool in a multi-tool fleet to meet a common specification-for-specification baseline, with tool-to-tool variation bound to levels that do not affect the downstream process. CEQ is achieved through structured tool-matching protocols executed at tool commissioning, after every maintenance event, and on a quarterly scheduled cadence. In semiconductor fabs, CEQ is considered foundational rather than optional.

#### ▸ Solar Cell Adaptation

The solar cell equivalent, fleet-wide tool baselining, is practiced in many solar fabs but not universally nor rigorously. The ES Foundry adaptation formally deployed the semiconductor CEQ discipline across all multi-tool process steps at the facility: 6 Diffusion/annealing furnaces, 9 PECVD machines, 4 screen printing lanes, 4 firing furnaces, 6 wet benches, and 4 flash-test stations. Every tool was individually characterized and baselined against a reference tool within its category, with tool-specific offsets captured and used for the subsequent fleet-matching protocol.

#### ▸ Outcome at ES Foundry

The CEQ discipline eliminated what would otherwise have been a multi-month tail of inter-tool yield variation. In the absence of CEQ, it is typical for solar cell ramps to see tool-to-tool yield spread of 5 to 12 percentage points that closes only slowly as engineering teams investigate and correct tool-specific offsets. With CEQ deployed from day one, tool-to-tool yield spread at ES Foundry was bounded to 1.8 percentage points at month 3 and 0.6 percentage points at month 9.

### 3.4 Discipline 4 - Process Integration Team Structure

#### ▸ Semiconductor Origin

In semiconductor backend, the process integration engineer (PIE) is a specific role whose responsibility is the engineering ownership of the interaction effects between successive process steps. The PIE is distinct from the process module engineer, who owns the performance of a single process step. While the module engineers ensure that each step meets its own specification, the PIE ensures that the combination of steps produces a high-yield final device. The PIE function requires broad device physics knowledge and systemic analytical capability.

**• Solar Cell Adaptation**

Solar cell manufacturing traditionally has less clearly delineated integration versus module engineering roles, with process engineers often owning both the single-step performance and the multi-step integration effects. The ES Foundry adaptation formally separated the two functions: eight process module engineering teams were established, each with clear ownership of a single process step; two process integration teams were established, each with cross-step ownership for the front-end (wafer through diffusion) and back-end (PECVD through flash test) process flows respectively.

**• Outcome at ES Foundry**

The separation of integration and module responsibility had an outsized effect on the speed at which cross-step yield issues were diagnosed. Issues such as the diffusion-profile-driven downstream metallization defect rate, or the junction-depth-driven electroluminescence signature variation, are inherently integration-layer problems that fall between the responsibilities of any single module team. At ES Foundry, 18 integration-layer issues were identified and resolved in the first 9 months; industry benchmark suggests these same issues would typically have been resolved over 12 to 18 months in facilities without formal integration engineering.

**3.5 Discipline 5 - EL-Based Defect Categorization System****• Semiconductor Origin**

The semiconductor backend relies heavily on automated optical inspection (AOI) with classifier-based defect categorization as the primary wafer-level quality gate. Modern semiconductor AOI systems apply pre-trained deep-learning classifiers to each image to bin detected defects into categories (particles, scratches, opens, bridges) at production throughput, enabling real-time Pareto analysis and process-step attribution without human review of most images.

**• Solar Cell Adaptation**

The solar cell analog is electroluminescence imaging with classifier-based categorization, but the maturity of solar EL classifier systems at 2025 is substantially less advanced than semiconductor AOI. The ES Foundry adaptation invested in the development of a custom EL classifier system using deep-learning models trained on the first 100,000 production cells, yielding a classifier that could automatically bin 94% of EL images into defined defect categories without human review.

**• Outcome at ES Foundry**

The EL classifier deployment was achieved by month 4 and immediately changed the cadence of yield engineering activity. Prior to classifier deployment, the yield engineering team reviewed approximately 800 EL images per day manually, an activity that consumed approximately 4 engineer-hours daily and could process only a small sample of total production. Post-classifier deployment, 100% of production EL images were automatically categorized and only anomalous cases (approximately 6% of images) required human review. The resulting increase in defect-detection coverage and attribution speed is a principal component of the Cpk trajectory.

**3.6 Discipline 6 - Run-to-Run Control****• Semiconductor Origin**

Run-to-run (R2R) control is the semiconductor discipline of using post-process metrology to automatically adjust the next-wafer recipe parameters via a feedback controller. R2R is distinct from both closed-loop in-situ control (which operates within a single wafer processing cycle) and periodic manual recipe adjustment (which operates at days-to-weeks cadence). R2R operates at wafer-to-wafer or lot-to-lot cadence and uses a PID or Kalman-filter controller tuned to the specific metrology-to-recipe coupling.

**• Solar Cell Adaptation**

The adaptation of R2R to solar cell context required substantive modification because the process-metrology coupling in solar manufacturing differs from semiconductor. In the semiconductor, R2R typically couples a post-etch critical dimension measurement back to the lithography exposure dose for the next wafer. In solar, the highest-leverage R2R application identified at ES Foundry was coupling the Back passivation uniformity to the TMA gas flow and RF power, with Kalman-filter controllers handling the expected drift and noise characteristics of the coupling.

**• Outcome at ES Foundry**

R2R control was deployed in a limited scope at month 6 and expanded to cover PECVD and diffusion processes by month 9. The R2R deployment is the principal driver of the within-lot Cpk improvement from 1.12 at month 3 to 1.67 at month 9, a result that classical Shewhart/CUSUM SPC alone would have achieved more slowly.

### 3.7 Discipline 7 - Printer Fleet Matching

#### • Semiconductor Origin

While semiconductor backend does not use screen printing per se, the analogous discipline is the inter-tool matching of litho-cluster tools, etch chambers, and deposition modules within a multi-chamber platform. The protocols used for matching multiple litho exposure stations or multiple etch chambers translate directly to the matching of multiple screen printing tools in solar cell context.

#### • Solar Cell Adaptation

The ES Foundry printer fleet matching protocol was adapted from semiconductor etch chamber matching and applied to the eight screen printing lines in the metallization module. The protocol characterized each printer against a reference unit via a standardized 300-wafer qualification run, computed line-specific linewidth, height, and alignment offsets, and applied corrective adjustments to squeegee angle, pressure, and stroke speed.

#### • Outcome at ES Foundry

The printer fleet matching protocol reduced inter-printer linewidth offset from an initial 3.4 micrometer range (at first-silicon) to a sustained 0.4 micrometer range (by month 6) - an 8.5x reduction that was a major contributor to metallization-module Cpk achievement.

### 3.8 Discipline 8 - DOE-Based Recipe Optimization

Design of experiments methodology transfers directly from semiconductor to solar with minimal adaptation. The discipline was deployed at ES Foundry without substantive modification and applied to 14 recipe optimization campaigns during the first 9 months of operation, spanning Texture, PECVD, diffusion, metallization, and firing recipes. Each DOE followed a structured framework of problem definition, factor screening, response surface characterization, confirmation trials, and formal recipe release. The systematic application of DOE, rather than the more common ad-hoc recipe tuning in solar industry practice, produced measurable recipe performance improvements.

### 3.9 Discipline 9 - PFMEA Methodology

Process failure mode and effect analysis (PFMEA), a discipline extensively used in both automotive and semiconductor manufacturing, was deployed at ES Foundry as the structured framework for systematically identifying and mitigating failure modes at each process step. The PFMEA output is a risk priority number (RPN) for each potential failure mode, computed as the product of severity, occurrence probability, and detectability ratings. Corrective actions are prioritized against the RPN ranking. The ES Foundry PFMEA program identified 187 distinct failure modes across the 8 process steps, of which 42 were classified as high-priority (RPN > 200), and of these 39 were mitigated through engineering controls by month 9.

“Borrowed disciplines are not borrowed identities. The solar cell factory does not become a semiconductor fab by adopting semiconductor practice - but it does become a factory that ramps faster, runs tighter, and reaches parity with mature competition on a materially shorter timeline.”

## IV. YIELD RAMP OUTCOMES AND METRICS

### 4.1 Line Yield Trajectory

The primary outcome metric of the knowledge transfer program is the line yield trajectory from first-silicon through stabilization. The ES Foundry line yield, defined as the percentage of incoming wafers that successfully complete all 8 process steps and meet or exceed minimum-bin cell efficiency specification, was measured weekly from first-silicon onward. The monthly summary is reported in Table 3.

TABLE 3 | Monthly line yield trajectory - ES Foundry first 9 months of operation

Month	Line Yield	Primary Loss Category	Benchmark (typical)
Month 1 (Feb 2025)	68.2%	Process integration issues	55-65%
Month 2 (Mar 2025)	76.4%	Metallization defects	62-70%

Month	Line Yield	Primary Loss Category	Benchmark (typical)
Month 3 (Apr 2025)	83.1%	Etching uniformity	68-75%
Month 4 (May 2025)	87.6%	Firing profile excursions	72-80%
Month 5 (Jun 2025)	90.3%	Edge isolation defects	76-82%
Month 6 (Jul 2025)	93.8%	PECVD thickness uniformity	80-85%
Month 7 (Aug 2025)	94.2%	Random metallization defects	82-86%
Month 8 (Sep 2025)	94.6%	Random metallization defects	83-87%
Month 9 (Oct 2025)	94.9%	Stable baseline - no dominant mode	84-88%

The ES Foundry trajectory consistently exceeded the industry benchmark for comparable greenfield solar cell ramps. The most consequential comparison is at month 5, where ES Foundry reached 90.3% line yield, a level that industry benchmark suggests is typically reached at months 9 through 11 for greenfield PERC facilities without a structured cross-technology knowledge transfer program. The absolute yield advantage at any given month was 7 to 13 percentage points above benchmark midpoints.

#### 4.2 Process Capability Trajectory

Process capability, measured as the Cpk index for each of 18 primary process parameters tracked in the SPC architecture, followed a trajectory that illustrates the differential contribution of the various transferred disciplines. The monthly summary of the mean Cpk across all 18 parameters, and the count of parameters achieving  $Cpk \geq 1.50$  each month, is reported in Table 4.

**TABLE 4 | Process capability (Cpk) trajectory - mean Cpk and count above 1.50 threshold**

Month	Mean Cpk	Params $\geq 1.50$	Params $\geq 1.67$	Benchmark (mean Cpk)
Month 1	0.82	2 of 18	0 of 18	0.70-0.85
Month 2	0.97	5 of 18	2 of 18	0.80-0.95
Month 3	1.12	8 of 18	4 of 18	0.88-1.05
Month 4	1.28	11 of 18	6 of 18	0.95-1.12
Month 5	1.42	13 of 18	8 of 18	1.02-1.18
Month 6	1.54	14 of 18	10 of 18	1.08-1.25
Month 7	1.61	15 of 18	11 of 18	1.13-1.30
Month 8	1.66	16 of 18	12 of 18	1.17-1.33
Month 9	1.70	17 of 18	13 of 18	1.20-1.36

By month 9, 17 of the 18 primary process parameters had achieved sustained  $Cpk \geq 1.50$ , representing effectively full-fleet process capability. The single parameter still operating below  $Cpk = 1.50$  is the flash-test efficiency uniformity across the flash-test station fleet, which is undergoing further tool-matching work targeted for Q1 2024.

#### 4.3 Overall Equipment Effectiveness

Overall Equipment Effectiveness (OEE), the composite productivity measure combining availability, performance, and quality, tracked alongside the yield and capability metrics. The OEE trajectory for the facility is summarized in Table 5.

TABLE 5 | Monthly Overall Equipment Effectiveness (OEE) trajectory

Month	Availability	Performance	Quality	OEE
Month 1	72%	81%	68%	40%
Month 3	84%	88%	83%	61%
Month 5	89%	92%	90%	74%
Month 6	91%	93%	94%	80%
Month 9	93%	95%	95%	84%

#### 4.4 Cost-Per-Watt Trajectory

The cost-per-watt trajectory, while heavily influenced by factors beyond engineering knowledge transfer (equipment amortization, silver paste pricing, labor rates, energy costs), nonetheless showed a clear correlation with the yield ramp. The monthly cost-per-watt against industry benchmark is summarized as follows.

–47% Cost-per-watt reduction from month 1 to month 9

14% Remaining cost gap to offshore incumbent benchmark by month 9

18 months Timeline advance versus pre-program cost-parity projection

\$0.036/W Absolute cost-per-watt at month 9 (blended facility cost)

### V. LESSONS LEARNED AND GENERALIZABLE INSIGHTS

#### 5.1 Validated Hypotheses

The knowledge transfer program as designed rested on several explicit hypotheses about the relationship between semiconductor practice and solar cell manufacturing. The following hypotheses are validated by the 9-month outcome data.

→ **H1 - Direct transferability of SPC:** The semiconductor SPC architecture transfers to solar context with minimal adaptation and delivers Cpk improvements comparable to those achieved in the source industry. VALIDATED: Mean Cpk trajectory exceeded benchmark by 30 to 40% at every measurement point.

→ **H2 - Value of pre-ramp SPC deployment:** SPC deployed before first-silicon produces faster yield ramp than SPC retrofitted after ramp. VALIDATED: ES Foundry reached 90% yield at month 5 versus benchmark 9 to 11 months.

→ **H3 - CEQ discipline transferability:** Copy-exact qualification transfers with moderate adaptation and eliminates the multi-month tool-matching tail typical of solar ramps. VALIDATED: Inter-tool yield spread closed to < 1 percentage point by month 6.

→ **H4 - PIE function independence:** Formal separation of process integration engineering from module engineering accelerates cross-step issue resolution. VALIDATED: 18 integration issues resolved in 9 months versus benchmark 12 to 18 months.

→ **H5 - EL classifier deployment value:** Automated EL defect classification at 100% coverage produces better yield outcomes than manual sampling. VALIDATED: Defect attribution speed improved 10x; yield engineering headcount enabled by the classifier was redirected to integration work.

#### 5.2 Partially Validated Hypotheses

Several hypotheses were partially validated, meaning the knowledge transfer produced measurable benefits but the magnitude or pace did not match the original expectations.

→ **H6 - R2R control deployment pace:** R2R control expected to be deployed within 120 days of first-silicon. ACTUAL: R2R deployed at day 180 for Etching tools only, with full deployment not completed until day 300. The pace was constrained by the modeling and validation effort required for each control loop.

→ **H7 - PFMEA-driven failure-mode coverage:** PFMEA expected to identify and prospectively mitigate 90% of failure modes before they manifested. ACTUAL: 39 of 42 high-priority failure modes were identified and mitigated pre-deployment, representing 93%, but several lower-RPN modes manifested that PFMEA had not prospectively captured.

→ **H8 - General manufacturing engineer learning curve:** Recruited general-manufacturing engineers expected to reach solar-specific proficiency within 90 days. ACTUAL: Mean time to solar-specific proficiency was 127 days, with

substantial individual variation. Knowledge transfer through mentorship from imported experts was the primary accelerator.

### **5.3 Observations Not Anticipated by the Original Plan**

Three observations emerged during the deployment that were not anticipated by the original program design.

**1. The semiconductor-to-solar PFMEA adaptation required more cultural adjustment than technical modification.** The formal risk scoring and corrective-action-tracking discipline of semiconductor PFMEA met initial resistance from solar-origin engineers accustomed to more informal issue tracking. Resolution required structured training in the PFMEA methodology combined with executive-level reinforcement of the process discipline, which was not anticipated in the original program resource plan.

**2. The communication protocols between process modules required explicit design.** Semiconductor facilities have well-established protocols for cross-module issue escalation, change management, and shared metrics reporting. Solar facility traditions proved less structured, and the ES Foundry program had to explicitly codify cross-module communication expectations early in the ramp to avoid siloed problem-solving that would have slowed integration issue resolution.

**3. The metrology-tool integration effort exceeded original estimates.** The heterogeneous metrology tool fleet (sheet resistance probes from one vendor, EL cameras from another, flash testers from a third) required substantially more data-integration engineering work than was scoped in the original plan. Approximately 2.4 engineer-years of integration effort was spent on metrology data pipelines against a pre-program estimate of 0.8 engineer-years.

### **5.4 Recommendations for Similar Future Programs**

Based on the ES Foundry experience, the following recommendations are offered to operators of future greenfield solar cell facilities (or, more broadly, operators of greenfield facilities in any adjacent manufacturing industry seeking to apply cross-industry knowledge transfer).

→ **Invest heavily in pre-first-silicon documentation:** Phase One codification work should not be treated as optional or deferrable. The value of deploying the transferred disciplines at first-silicon rather than retrofitting them is the single largest lever in the entire program.

→ **Staff with explicit cross-industry composition:** Neither a solar-only nor a semiconductor-only engineering staff will produce the optimal outcome. The deliberate staffing of the yield-ramp team with both imported and native expertise creates the analytical friction that surfaces insights neither tradition would independently produce.

→ **Build the EL classifier early:** The automated EL classifier is arguably the single highest-impact engineering tool in a modern greenfield solar cell facility. Early investment in classifier development, preferably beginning during the tool move-in period, will accelerate yield engineering productivity substantially.

→ **Formalize process integration engineering:** Cross-step issues are the hardest to find and the slowest to resolve. The PIE function should be explicitly staffed and resourced rather than left as an implicit shared responsibility of module teams.

→ **Scope metrology integration realistically:** Metrology data integration effort is consistently under-estimated. Scope the MES-metrology integration work at approximately 3x the naive estimate based on count of metrology tools - this is a pattern observed in both semiconductor fab commissioning literature and replicated at ES Foundry.

## **VI. CONCLUSIONS AND FORWARD AGENDA**

This paper has documented the design and execution of a structured cross-technology engineering knowledge transfer program at ES Foundry's US-domestic solar cell manufacturing facility in Greenwood, South Carolina. The program transferred 9 distinct engineering disciplines from semiconductor backend manufacturing practice into the solar cell manufacturing context, with formal codification, adaptation, and deployment phases executed between October 2024 and October 2025. The measurable outcomes - line yield of 94.9% by month 9 versus industry benchmark of 84 to 88%, mean Cpk of 1.70 versus benchmark of 1.20 to 1.36, OEE of 84% versus benchmark of 72 to 78%, and cost-per-watt convergence 18 months ahead of pre-program projection - support the broader claim that structured cross-industry knowledge transfer is not merely an academic exercise but a material lever on commercial outcomes in greenfield manufacturing.

The principal generalizable finding is that the value of cross-technology knowledge transfer comes not from treating the source and destination industries as interchangeable, but from systematically identifying which disciplines transfer directly, which require specific adaptation, and which simply do not transfer at all. This triage is the core intellectual

work of the knowledge transfer program, and it is the work that cannot be shortcut. The semiconductor SPC architecture transferred with near-zero adaptation and delivered substantial benefit; the semiconductor R2R control discipline transferred with substantial adaptation and delivered moderate benefit over a longer timeline; some semiconductor disciplines were evaluated and explicitly chosen not to be transferred because the adaptation cost would have exceeded the anticipated benefit in the solar context.

### 6.1 Forward Agenda

The knowledge transfer program at ES Foundry continues into 2026 and 2027 with three focused workstreams.

→ **Workstream 1 - Second-line deployment:** The disciplines validated on the first GW line will be deployed to the second GW line (commissioned Q1 2026) with the expectation of faster ramp (target: 7 months to 94% line yield versus 9 months on first line) by virtue of the mature discipline playbooks and trained engineering workforce.

→ **Workstream 2 - Discipline-specific deepening:** The R2R control discipline will be deepened through expansion of the control loop set to additional process steps. The PFMEA discipline will be extended to include customer-use-case failure modes beyond the process-step modes covered in 2025.

→ **Workstream 3 - Next-generation technology preparation:** The Next technology transition scheduled for 2029-29 will leverage the established disciplines as its baseline, with the knowledge transfer methodology itself being the vehicle for the yield ramp. The expected ramp compression from applying the discipline playbook to next Technology would be 30 to 40% faster than PERC was.

The broader institutional learning - that systematic knowledge transfer from adjacent manufacturing industries is an accelerator of greenfield ramp, not merely a nicety - is expected to be applicable to future facility projects in the US domestic solar manufacturing base as that base matures in response to sustained policy support.

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